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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/820,182	04/08/2004	Tsutomu Sato	04329.3299	7391

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EXAMINER	
KRAIG, WILLIAM F	

ART UNIT	PAPER NUMBER
2815	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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Office Action Summary	Application No.	Applicant(s)	
	10/820,182	SATO ET AL.	
	Examiner	Art Unit	
	William Kraig	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 April 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15 and 21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,14 and 21* is/are rejected.

7)☒ Claim(s) *3,5-13 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/19/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1, 2, 4, 14 and 21 are rejected under 35 USC § 102(b) as being anticipated by U.S. Patent Publication No. 2002/0076865 to Dennison et al.

With regards to claim 1, Figs. 2-22 of Dennison et al. illustrate a semiconductor substrate ((area below 34), (area filled by 44), 40, 42, 38, 46, 54 and 56) including a main surface (upper surface of 56);

a MOSFET including a double gate structure (50 and 60) provided on a side of the main surface of the semiconductor substrate (see Figs. 2-22), the double gate structure comprising top 60 and bottom 50 gate electrodes, the bottom gate electrode 50 being located at a lower level than the main surface (see Figs. 2-22); and

an isolation region 44 for isolating the MOSFET from other elements comprising a trench (trench is the area in which isolation region 44 is formed) provided on the side of the main surface of the semiconductor substrate and an insulator 44 provided in the trench, the isolation region 44 having a region (a region of the isolation region is disposed on the right side of both Fig. 13 and Fig. 14, said region being the portion of 44 directly beneath bottom gate electrode 50) in the trench around the MOSFET (see Figs. 13 and 14), the region (the above described region) having a deeper bottom than

other regions in the trench (it can be seen in Figs. 13 and 14 that the above described region of insulator 44 extends deeper into the substrate than a different portion of isolation region 44, said different portion being on the left side of both Fig. 13 and Fig. 14 and being directly above layers 38), and all of the region having the deeper bottom (a region of the isolation region is disposed on the right side of both Fig. 13 and Fig. 14, said region being the portion of 44 directly beneath bottom gate electrode 50) being covered with the top gate electrode (see Fig. 13).

Regarding claim 2, Dennison et al. discloses the semiconductor device of claim 1, wherein the bottom gate electrode 50 is provided in the semiconductor substrate (see Figs. 2-22);

a part of the side of the main surface of the semiconductor substrate (upper surface of 56) is placed between the top gate electrode 60 and bottom gate electrode 50 (see Figs. 13 and 14), and the MOSFET further comprises:

a top gate insulating film 58 (see Fig. 7) provided between the top gate electrode 60 and the semiconductor substrate (see Fig. 7); and

a bottom gate insulating film 54 provided between the portion of the semiconductor substrate below the top gate electrode (56) and the bottom gate electrode (50).

Regarding claim 4, Figs. 2-22 of Dennison et al. disclose a semiconductor substrate ((area below 34), (area filled by 44), 40, 42, 38, 46, 54 and 56));

a MOSFET including a double gate (50 and 60) structure comprising top 60 and bottom 50 gate electrodes and provided on the semiconductor substrate (see Figs. 2-22); and

an isolation region 44 for isolating the MOSFET from other elements comprising a trench (trench is the area in which isolation region 44 is formed) provided on the side of the main surface of the semiconductor substrate and an insulator 44 provided in the trench, the isolation region 44 having a region (a region of the isolation region is disposed on the right side of both Fig. 13 and Fig. 14, said region being the portion of 44 directly beneath bottom gate electrode 50) in the trench around the MOSFET (see Figs. 13 and 14), the region (the above described region) having a deeper bottom than other regions in the trench (it can be seen in Figs. 13 and 14 that the above described region of insulator 44 extends deeper into the substrate than a different portion of isolation region 44, said different portion being on the left side of both Fig. 13 and Fig. 14 and being directly above layers 38), and all of the region having the deeper bottom (a region of the isolation region is disposed on the right side of both Fig. 13 and Fig. 14, said region being the portion of 44 directly beneath bottom gate electrode 50) being covered with the bottom gate electrode (see Fig. 13),

wherein the semiconductor substrate ((area below 34), (area filled by 44), 40, 42, 38, 46, 54 and 56)) is provided with at least one empty space (space in substrate filled by bottom gate electrode 50 and gate insulator 54), and the bottom gate electrode 50 and a bottom gate insulating film 54 are provided in the at least one empty space (see Figs. 2-22).

Regarding claim 14, Dennison et al. discloses the semiconductor device according to claim 4, wherein the at least one empty space (space in substrate filled by bottom gate electrode 50 and gate insulator 54) comprises an upper wall (bottom of 54) which includes a flat region (see Fig. 19).

Regarding claim 21, Dennison et al. discloses the semiconductor device according to claim 1, wherein the whole of the region having the deeper bottom (a region of the isolation region is disposed on the right side of both Fig. 13 and Fig. 14, said region being the portion of 44 directly beneath bottom gate electrode 50) is located under the top gate electrode (it can be seen in Figs. 13 and 14 that the above described portion of insulator 44 is located at a level that can be described as being under the level at which the top gate electrode 60 is disposed).

Response to Arguments

2. Applicant's arguments with respect to all claims have been considered but are moot in view of the new ground(s) of rejection.

Allowable Subject Matter

3. Claims 3, 5-13 and 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for allowance:

Regarding claim 3, the closest prior art does not teach the MOSFET further comprising a side gate electrode and a side gate insulating film provided in the region having the deeper bottom than the other regions in the trench around the MOSFET, and a part of the insulator being provided in the region having the deeper bottom than the other regions under the side gate electrode in combination with the additionally claimed features, as is claimed by the Applicant. Thus, the Applicant's claim is determined to be novel and non-obvious.

Regarding claims 5-12 and 15, the closest prior art does not teach the trench opening a part of an upper wall of an at least one empty space, and a side gate insulating film and a side gate electrode being provided on a side of the semiconductor substrate on the at least one empty space opened by said trench in combination with the additionally claimed features, as is claimed by the Applicant. Thus, the Applicant's claim is determined to be novel and non-obvious.

Regarding claim 13, the closest prior art does not teach a part of the at least one empty space remaining unfilled by the bottom gate electrode and the bottom gate insulating film in combination with the additionally claimed features, as is claimed by the Applicant. Thus, the Applicant's claim is determined to be novel and non-obvious.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Jang ('979 and '044), Yoon et al. (2006/0134868), Chan et al. ('132 and '101), Bryant et al. ('807), Solomon et al. ('331) and Parke (2002/0192911).

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William Kraig whose telephone number is 571-272-8660. The examiner can normally be reached on Mon-Fri 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

WFK
06/19/2007

EUGENE LEE
PRIMARY EXAMINER